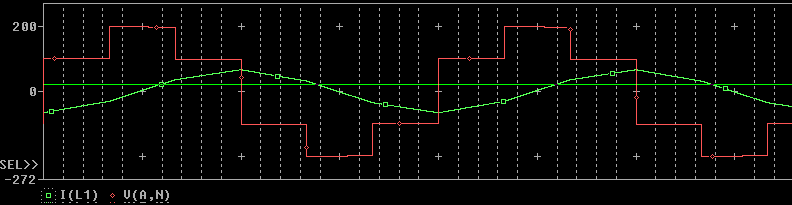
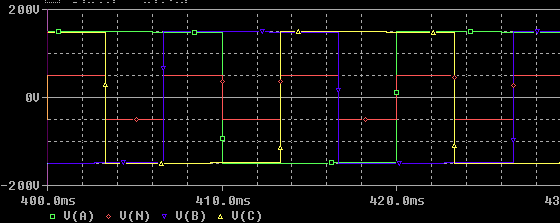
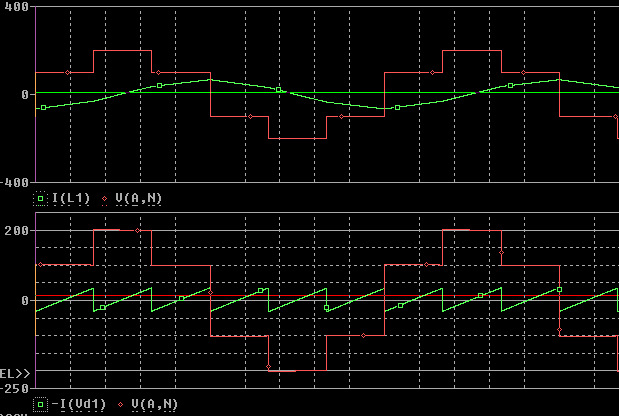
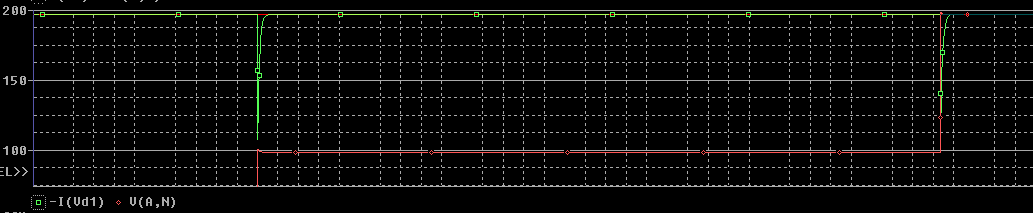
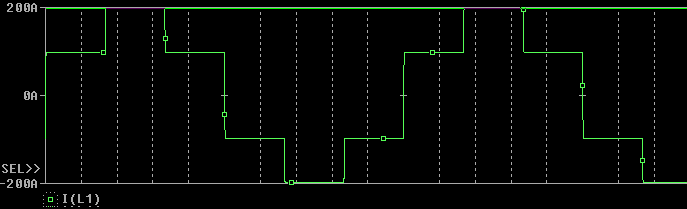
ENM061 – Lab 5 – 2019-12-19

1. The schematic models an RL-load with dominant inductance and marginal resistance. The resulting curves agree well with that of the purely inductive load. See HA1.

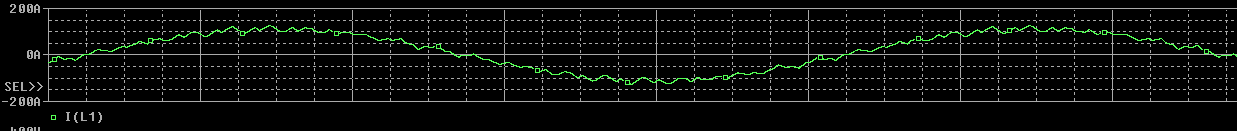
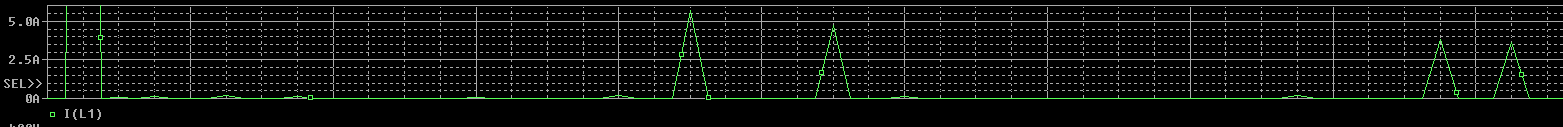
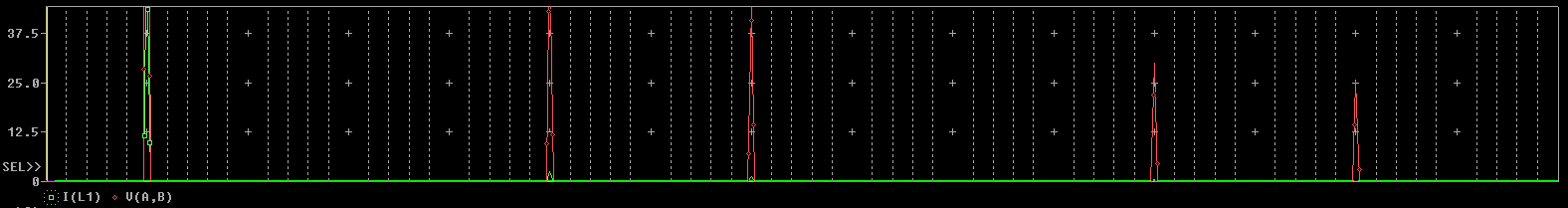
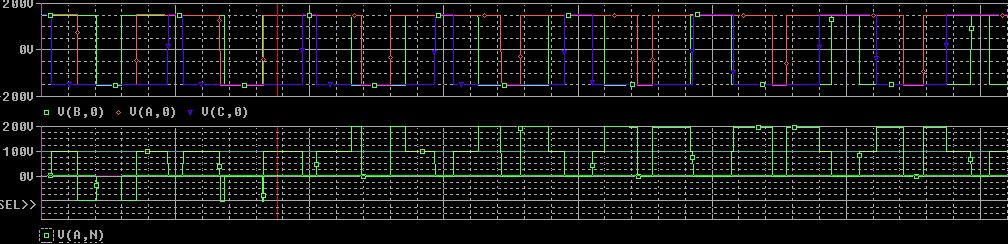
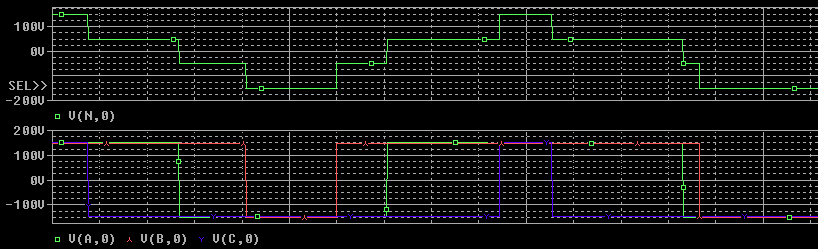
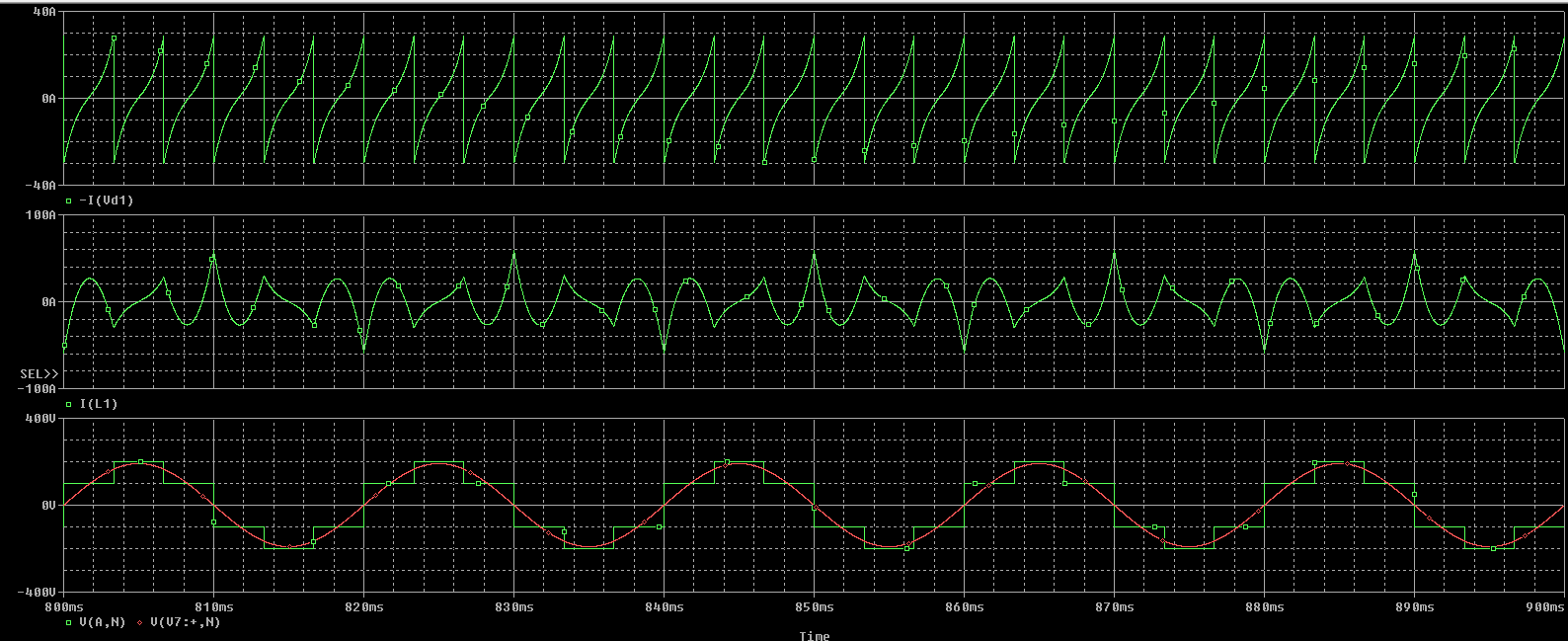


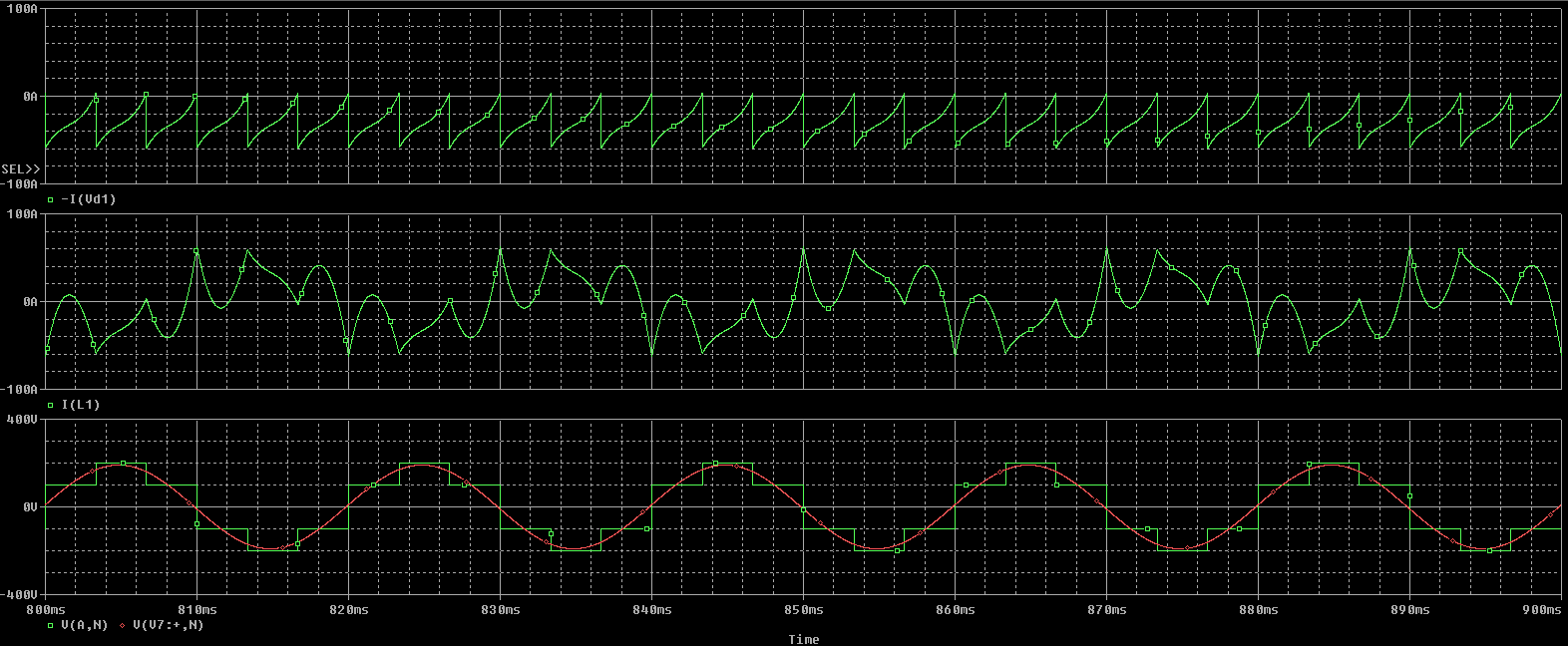
1. The voltage V\_4-0 (neutral to ground) was derived to be ).  
   In this case, each phase voltage V\_x-0 is at pos/neg Vd, depending on where in the cycle the system is. Invariably, two phases will be equal while the third is inverted.   
   As Vd=150V, the neutral point will always be some variant of 1/3\*(2\*150V + (-150V)) = +-50V  
     
   The plot backs up this assertion.  
   
2. Initial DC-input current is a sawtooth wave (-30A, 35A), f=50Hz\*6=300Hz.  
   After changing to L=10uH, R=1ohm : Constant current (197A) apart from when switching, which causes inductive spiking in (reverse)voltage and a consequent momentary reduction in input current.   
     
   Nominal values (10mH, 0.1ohm)  
   

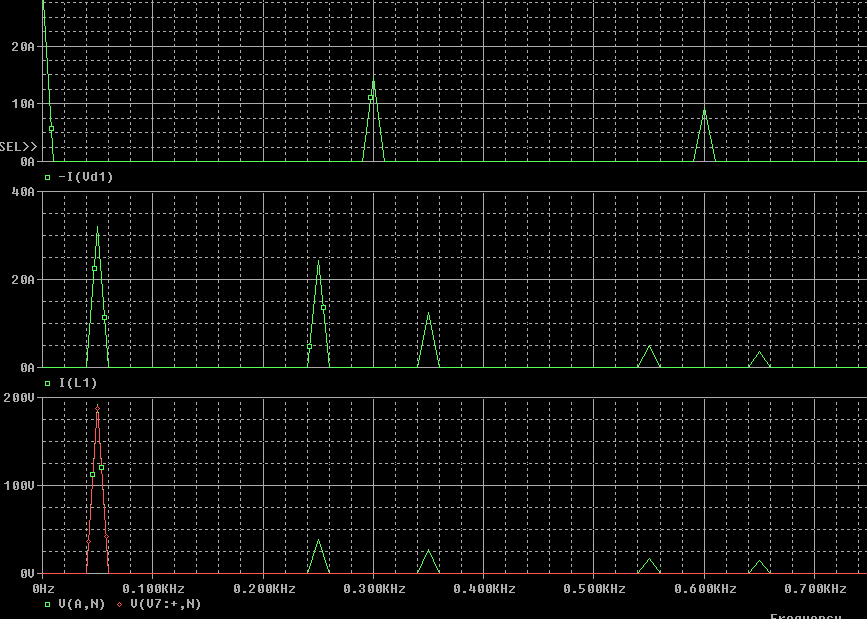
Changed values (10uH, 1ohm)  
  


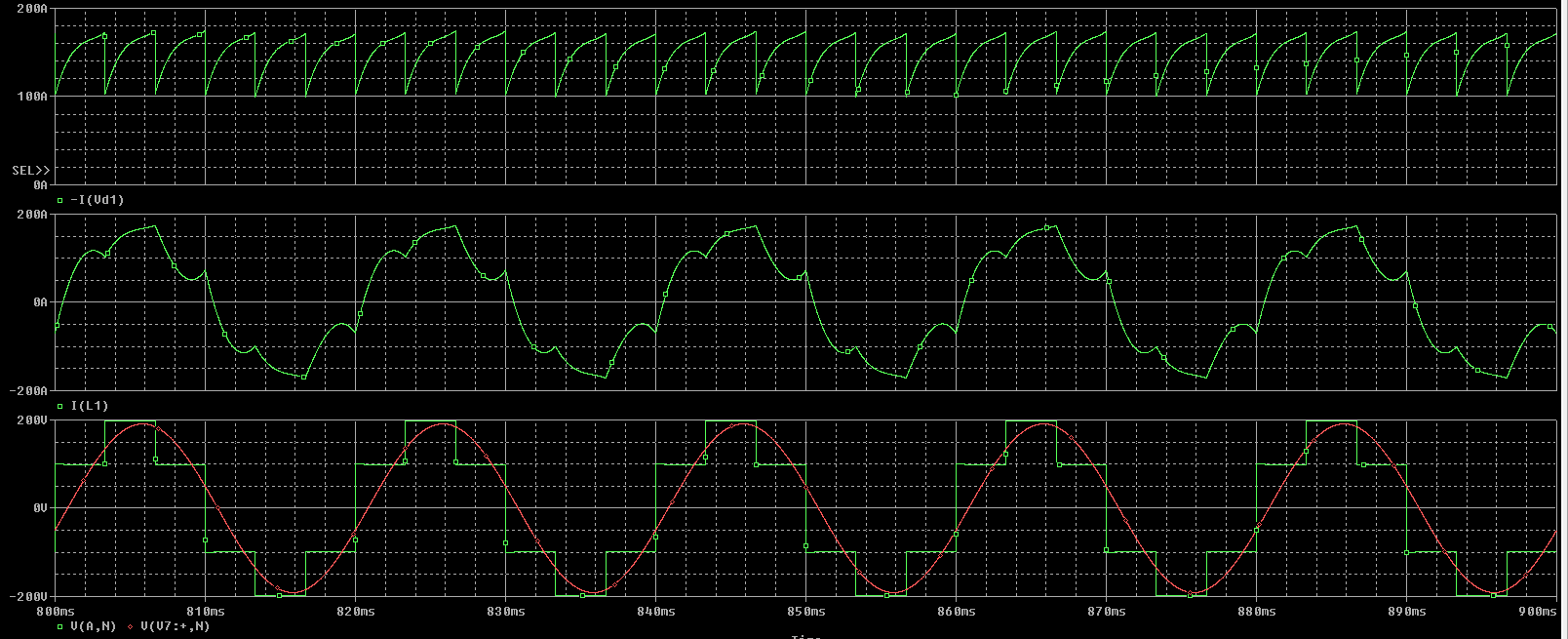
In the first case, the average input current (id) is only slightly positive and thus a small amount of active power is transferred to the load.

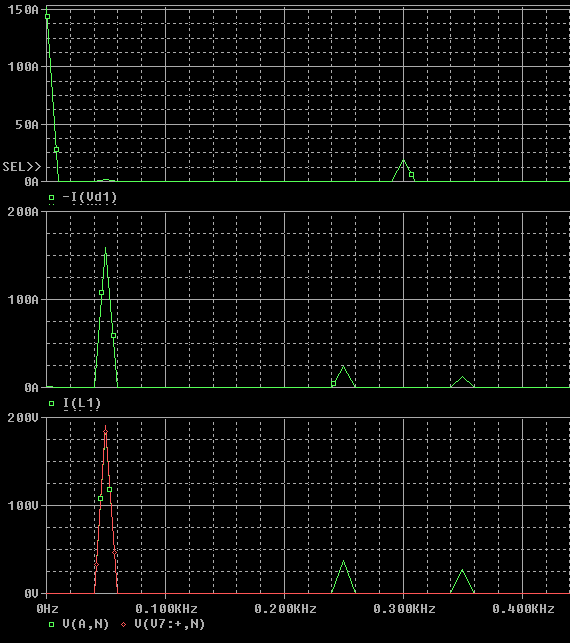
In the second case, the average current is approximately constant and positive and so almost all power transfer (to the load) is active. The output current waveform conforms well to that of the purely resistive load. See HA1.

1. PWM Modulated inverter  
     
     
     
   For PWM modulation  
   Mf = 1kHz/50Hz = 20  
   Harmonics at:  
   Odd Mf+-2  
   Even Mf+-1  
   Suppressed harmonic at Mf.  
     
   Follows harmonic content of V\_LL.  
     
   For Square wave modulation  
   Harmonics at:  
   6n+-1, where n is harmonics of f\_1 (the fundamental freq 50Hz)  
     
   Follows harmonics of V\_LL.  
   
2. The phase voltage was derived as (for a purely inductive load)This is observed to be correct.  
     
     
     
     
     
     
     
     
     
   The neutral (y-point) should still conform to the expression   
     
   Which it clearly does, just as in Q2.
3. If we assume that the back-emf is the same phase and magnitude as the fundamental output voltage, then they will cancel and the fundamental voltage (and thus current) component will be 0.  
   This also explains why only the characteristic ripple current remains (middle plot).  
   The ripple has an average value of 0 in steady state.  
   Thus, if the load has an average current of 0 across it, the average input current (DC component of id) must also be 0.  
     
   Only v\_A1 and i\_o1 are responsible for power transfer, and since i\_o1=0 the active power transfer is also 0.  
     
   

+3deg  


  
The output voltage and back-emf are now slightly out of phase, and so the phase voltage will not be cancelled out, leading to an average power transfer.  
This is clearly seen due to the fact that io1 now has a substantial value, and the DC component of id is consequently also large.  
Graphically, we can see that the average input current is negative and so active power must be transferred FROM the load.

-15deg  


  
The reasoning for this case is similar to the previous one.  
The main differences are that the average input current is now positive and so active power must be transferred TO the load, and that both id0 and io1 are much larger due to the greater back-emf phase-offset.